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5 **Method of Fabricating an Amorphous or Polycrystalline
Layer on an Insulating Region.**

BACKGROUND OF THE INVENTION.

10 1. Field of the Invention.

The invention, in general, relates to a method of fabricating an amorphous or polycrystalline layer on an insulating region and, more particularly, to a method of fabricating a semiconductor component with an improved amorphous or polycrystalline silicon germanium layer over an
15 insulating region.

In semiconductor technology amorphous or polycrystalline layers are applied in vastly different fields.

20 An important field of application of such layers is vertical bipolar transistors for high speed applications which, after mono-poly-silicon technology, may be fabricated with epitaxially incorporated base layers. Owing to the poor seeding of the conventional SiO₂-layer used as an insulating layer, the amorphous or polycrystalline silicon layer is usually
25 thinner than an epitaxially grown layer. Furthermore, homogeneous precipitation is made difficult by the poor and irregular seeding of the SiO₂-layer. In the case of polycrystalline silicon, grains of different sizes are formed which leads to a rough surface and irregular electrical properties. The problems increase drastically if instead of Si, SiGe or SiGe:C is being used.
30 In such cases, when precipitating the epitaxial layer seeding is so bad that no polycrystalline or amorphous precipitation on the SiO₂ is possible within the

time usually required for the precipitation of the epitaxial layer.

As regards the thickness of the epitaxial layer, there are two different requirements. Within the region of the emitter the thickness of the layer
5 between the highly doped emitter and the base should be sufficiently thin. In the area of the outer base, a greater thickness is advantageous to provide for low resistance of the base connector.

PATENT ABSTRACTS OF JAPAN, Vol. 012, No. 207 (E-621), 14 June
10 1988 (1988-06-14) & JP 63006874 A (FUJITSU LTD), 12 January 1988 (1988-01-12) and PATENT ABSTRACTS OF JAPAN, Vol. 011, No. 217 (E-523), 14 July 1987 (1987-07-14) & JP 62036865 A (FUJITSU LTD), 17 February 1987 (1988-01-12) in particular, disclose semiconductor components which contain a substrate, a SiO_2 layer, a Si_3Ni_4 layer on the
15 SiO_2 layer, a polycrystalline silicon layer on the Si_3Ni_4 layer and an epitaxial silicon layer applied on the substrate simultaneously with the polycrystalline silicon layer.

OBJECT OF THE INVENTION.

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It is an object of the invention to propose a method of fabricating an amorphous or polycrystalline silicon germanium layer on an insulating region by which, in contrast to methods hitherto used, the thickness of the amorphous or polycrystalline layer is greater, the homogeneity of the
25 precipitation is improved and the roughness of the surface is thus reduced. At the same time, the insulating properties of the insulating region are at least to be maintained.

BRIEF SUMMARY OF THE INVENTION.

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In accordance with the invention, the object is accomplished by

improving the seeding during precipitation of the amorphous or polycrystalline silicon germanium layer by applying a suitable seeding layer of good seeding capacity and insulating properties on the insulating region. As a result, the thickness of the amorphous or polycrystalline layer is significantly greater
5 than it would be in the absence of a seeding layer. The greater thickness of the amorphous or polycrystalline layer is obtained by improved seeding which leads to shortening of the induction period (idle time) for the precipitation on the insulating layer. The better and more uniform seeding of the seeding layer leads to a homogenous precipitation. This leads to uniform electrical
10 properties. Using a SiO₂-layer as an insulating layer and a silicon nitride layer as a seeding layer is particularly suitable.

DESCRIPTION OF THE SEVERAL DRAWINGS.

15 The novel features which are considered to be characteristic of the invention are set forth with particularity in the appended claims. The invention itself, however, in respect of its structure, construction and lay-out as well as manufacturing techniques, together with other objects and advantages thereof, will be best understood from the following description of preferred
20 embodiments when read in connection with the appended drawings, in which:

Fig. 1 is a schematic presentation of a bipolar transistor;

Fig. 2 is a schematic presentation of a bipolar transistor according to Fig. 1 during its fabrication;

25 Fig. 3 is a schematic presentation of a layer structure before epitaxy; and
Fig. 4 is a schematic presentation of a layer structure following epitaxy.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS.

30 Example 1:

The invention will now be described in connection with a mono-poly-

silicon process.

Fig. 1 schematically depicts a bipolar transistor 10. A collector region of conductivity type II has been fabricated on a semiconductor substrate region 11 of conductivity type I. If emitter and collector are, for instance, n-conductive, the base is type p, and *vice versa*. Several processes are known which provide for suitable collector doping. Among these is, for instance, the structure shown in Fig. 1 with a highly doped buried layer 12 and a less doped epitaxial layer 13 as well as implanted retrograde well. In the example shown, field insulating region 14 separates the bipolar transistor from other components not shown in the drawing and the collector connection region from the active region of the transistor. Other suitable insulating techniques are also known, such as, for instance, spaced mesa arrangements. In this example, a buried implant 20 has been incorporated to reduce the resistance between the highly doped contact layer 21 made of poly-silicon and the buried layer 12. In accordance with the invention, a layer 28 of excellent seeding capacity and insulating properties (seeding layer) is present on the insulating region. In the present embodiment, the layer 28 consists of silicon nitride.

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An epitaxial layer sequence consisting of a buffer layer 15, an *in situ* doped base layer 16 of conductivity type I as well as a cover layer 17, are covering the emitter region in the active transistor region and at least a section of the insulating region covered by the seeding layer 28. The epitaxial layer structured outside of the active transistor region is covered by a non-conductive material 18.

The use of a thick polycrystalline layer on the insulating region is to be considered as essential in the context of the invention. The specific values of the thickness, the dopant content as well as the material composition of the base are to be set in accordance with the requirements of the function of the

bipolar transistor and, in accordance with the invention, they are not subject to any special requirements. In the example shown, the base layer consists of silicon, is p-doped with $2 \cdot 10^{18} \text{ cm}^{-3}$ and is assumed to have a thickness of 40 nm. However, other material compositions and doping profiles may be
5 used as well. It is possible to use a thin cover layer 17 over the base layer. Doping of the emitter in the mono-silicon is ensured by outdiffusion of dopant 22 from the highly doped poly-silicon contact layer 21. The precipitated thickness of the cover layer 17 typically is 50 nm.

10 Whilst the buffer, base and cover layer grow monocrystalline over the silicon substrate, polycrystalline layers 19 are formed over the insulating region 14 provided with the seeding layer 28. In accordance with the invention, the thickness of the precipitated polycrystalline layer is increased by the use of the seeding layer 28. Outside of the poly-silicon contact layer
15 21 overlapping the active transistor region doping in the base connection region has been additionally increased by implantation 23. The insulating layer 24 separates emitter, base and collector contact. The transistor structure is completed by the metal contacts for emitter 25, base 26 and collector 27.

20 The fabrication of a bipolar transistor in accordance with the invention will be described hereafter. The method in accordance with the invention proceeds on the basis of the structure shown in Fig. 2. Following photolithographic structuring, a highly doped n-layer 12 is incorporated by
25 implantation in the p-doped silicon substrate 11, and annealed. Thereafter, a weakly doped n-layer 13 is precipitated epitaxially. The active region is defined by conventional process steps and generate insulating regions 14 (e.g. LOCOS) in the remaining regions. In accordance with the invention, a seeding layer 28 is precipitated over the whole surface and is opened over
30 the active transistor region. Preferably, silicon nitride is used for the seeding layer 28. The buffer layer 15, the base layer 16 and the cover layer 17 are

precipitated by means of differential epitaxy. By the use of the seeding layer 28 seeding of the insulating region is improved. In this manner the idle time for the precipitation on the insulating region is reduced. As a result, the polycrystalline layer 19 on the insulator is substantially thicker than it would be by precipitation without using the seeding layer 28.

After photolithographically structuring a mask the precipitated silicon or poly-silicon layers outside of the transistor and base connection region on the insulating region 14 are removed by a plasma etching step and an etching stop. Thereafter, a non-conductive material 18, preferably oxide, is applied.

By photolithographically structuring a lacquer mask the collector connection region will now be exposed and the buried implant 20 will be applied. After the lacquer mask has been removed and after structuring of a further lacquer mask, the oxide layer 18 is chemically wet etched in the collector connection region as well as in the emitter region. The process is continued by precipitation of an amorphous silicon layer. This may be doped by implantation *in situ*, during or following the precipitation. Emitter and collector contact regions are masked by a lithographic step. In the remaining regions, the amorphous silicon is removed by a plasma etching step with a stop on the SiO₂ layer. During the ensuing implantation of the base connection regions the emitter and collector contact regions are protected by the present masking. Tempering will take place after removal of the mask and covering of the generated surface with oxide for annealing the implantation defects and for forming the poly-emitter. The process is completed by opening the via holes for emitter, base and collector and by a standard metallization of the transistor contacts.

Example 2:

The basis for the method in accordance with the invention in this embodiment is the layer structure before epitaxy shown in Fig. 2. An

insulating layer 31 consisting of SiO_2 has been precipitated on silicon substrate 30 and has been structured by means of photolithographic processes. In accordance with the invention the insulating layer 31 is additionally partially covered by a structured seeding layer 32 consisting of silicon nitride. As shown in Fig. 4, the result of the epitaxy step is the generation of a mono-crystalline layer on uncovered silicon substrate. The polycrystalline layers 33 grown on the insulating layer 31 and seeding layer 32 are different in structure and thickness. Compared to the polycrystalline layer 33 on the insulating layer 31 the polycrystalline layer 33 on the seeding layer 32 is of a more homogenous and more finely grained structure and of greater thickness.

On the basis of concrete embodiments there has been described, in the context of the present invention, a method of fabricating an amorphous or polycrystalline layer on an insulating region. It is, however, to be mentioned that the present invention is not limited to the details of the embodiments of the specification since changes and alterations are being claimed within the scope of the claims.

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